WHAT IS CLAIMED IS:

1. A functional block comprising:

a system bus synchronizing with a system clock;

a functional circuit synchronizing with a local clock; and

a synchronizing circuit for determining the operation timing for signal exchange between said system bus and said functional circuit, wherein

said synchronizing circuit takes in said system clock and said local clock and determines said operation timing by determining the access time of said functional circuit from said system clock.

2. The functional block according to claim 1, wherein said synchronizing circuit takes in said system clock and said local clock and determines said operation timing by creating an access end signal for said functional circuit from said system clock.

3. The functional block according to claim 2, wherein said access end signal is created by using a counter actuated in synchronization with said system clock and a comparing circuit to compare the output of said counter with a frequency specifying signal.

4. The functional block according to claim 1, wherein said synchronizing circuit determines the operation timing for signal exchange between said system bus and said functional circuit, regardless of the type of said system bus.

5. The functional block according to claim 1, wherein the frequency of said system clock is not fixed to a specific frequency.

6. The functional block according to claim 1, wherein the frequency of said system clock is given to create design data at a register transfer level automatically.

7. A functional block comprising:

a system bus synchronizing with a system clock;

a functional circuit synchronizing with a local clock; and

a synchronizing circuit for determining the operation timing for signal exchange between said system bus and said functional circuit, wherein

said functional circuit and said synchronizing circuit are integrated into an entity.

8. The functional block according to claim 7, wherein said synchronizing circuit determines the operation timing for signal exchange between said system bus and said functional circuit, regardless of the type of said system bus.

9. The functional block according to claim 7, wherein the frequency of said system clock is not fixed to a specific frequency.

10. The functional block according to claim 9, wherein the frequency of said system clock is not fixed to a specific frequency as a result of the input of a

frequency specifying signal to said synchronizing circuit.

11. A semiconductor integrated circuit including:

a system bus synchronizing with a system clock;

a functional circuit synchronizing with a local clock; and

a synchronizing circuit for determining the operation timing for signal exchange between said system bus and said functional circuit, wherein

said synchronizing circuit takes in said system clock and said local clock and determines said operation timing by determining the access time for said functional circuit from said system clock.

12. The semiconductor integrated circuit according to claim 11, wherein said synchronizing circuit takes in said system clock and said local clock and determines said operation timing by creating an access end signal for said functional circuit from said system clock.

13. The semiconductor integrated circuit according to claim 12, wherein said access end signal is created by using a counter actuated in synchronization with said system clock and a comparing circuit to compare the output of said counter with a frequency specifying signal.

14. The semiconductor integrated circuit according to claim 11, wherein said synchronizing circuit

determines the operation timing for signal exchange between said system bus and said functional circuit, regardless of the type of said system bus.

15. The semiconductor integrated circuit according to claim 11, wherein the frequency of said system clock is not fixed to a specific frequency.

16. The semiconductor integrated circuit according to claim 11, wherein the frequency of said system clock is given to create design data at a register transfer level automatically.

17. A semiconductor integrated circuit including:

a system bus synchronizing with a system clock;

a functional circuit synchronizing with a local clock; and

a synchronizing circuit for determining the operation timing for signal exchange between said system bus and said functional circuit, wherein

said functional circuit and said synchronizing circuit are integrated into a functional block.

18. The semiconductor integrated circuit according to claim 17, wherein said synchronizing circuit determines the operation timing for signal exchange between said system bus and said functional circuit, regardless of the type of said system bus.

19. The semiconductor integrated circuit according to claim 17, wherein the frequency of said system clock is not fixed to a specific frequency.

20. The semiconductor integrated circuit according to claim 19, wherein the frequency of said system clock is not fixed to a specific frequency as a result of the input of a frequency specifying signal to said synchronizing circuit.